Avago Demonstrates Industry-Leading 56Gbps PAM4 SerDes

January 6, 2015

Customers Now Designing in Avago PAM4 Transceivers Across Copper Backplane, Direct-Attached Cables and Optics, Doubling System IO Bandwidth

SAN JOSE, Calif., and SINGAPORE, Jan. 6, 2015 (GLOBE NEWSWIRE) -- Avago Technologies (Nasdaq:AVGO) today announced it has demonstrated the industry's first 56Gbps pulse-amplitude modulation (PAM)4 SerDes across copper backplanes and optical interconnects targeting next-generation switches and routers. Leading OEM customers are presently designing advanced ASIC SoC solutions in 28nm and 16FF+ process technologies utilizing the Avago PAM4 SerDes cores.

PAM4 technology enables future scaling of core/metro router and hyperscale data centers by more than doubling link full-duplex throughput to 56Gbps from 25Gbps per SerDes lane. Rack-level applications will particularly benefit from PAM4 technology realizing advantages in space, power, cost, and simplified cabling.

"Avago is proud to deliver the industry's first PAM4 56Gbps SerDes that ushers in a new era of SerDes interconnect technology for networking applications," said Frank Ostojic, Avago senior vice president and general manager, ASIC Products Division. "Our customers, many of whom have come to regard Avago's industry-leading SerDes as industry-standard, are utilizing the PAM4 SerDes cores to design best-in-class ASIC solutions to meet the explosive bandwidth growth in datacenter and service provider networks."

The Avago 56Gbps PAM4 SerDes is designed to support a wide range of copper and optical interconnects ranging from chip-to-chip, chip-to-module, low-cost direct-attached cable, and copper backplane down to 35dB loss. The SerDes supports speeds from 1Gbps to 56Gbps, including existing 10G/25G/40G/50G/100G Ethernet, Fibre Channel, and OIF CEI NRZ speeds, providing investment protection and a forward-looking architecture path to networking, compute system vendors, and mega data center companies.

By also targeting emerging OIF CEI-56G-VSR and IEEE 802.3bs (400GE) electrical standards defining next generation chip-to-module interconnect, the Avago 56Gbps PAM4 SerDes provides the additional benefit of enabling the same PAM4 signaling deployment on front side and back side interfaces, thus increasing SoC use case flexibility and reusability across hardware platforms.

The Avago 56Gbps PAM4 SerDes, now available in silicon, is running PRBS31 traffic, error-free, across various interconnects up to 56Gbps, thus reducing ASIC development risk and accelerating Avago customer system deployment.

About Avago Technologies

Avago Technologies is a leading designer, developer and global supplier of a broad range of analog, digital, mixed signal and optoelectronics components and subsystems with a focus in III-V compound semiconductor design and processing. Backed by an extensive portfolio of intellectual property, Avago products serve four primary target markets: wireless communications, wired infrastructure, enterprise storage, and industrial and other. For more information, visit Avago's website: www.avagotech.com.

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