Success in Custom Silicon Accelerators

Broadcom and Deutsche Bank Custom Silicon Teach-In
April 19, 2022
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Broadcom Speakers

Hock E. Tan
President & CEO

Frank Ostojic
SVP & GM, ASIC Products

Vijay Janapaty
VP & GM, Physical Layer Products
How Broadcom Became a Global Technology Leader
Category-Leading Franchises: 8 in 2009 → 22 Today

Revenue
($ in Billions)

18X Growth

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<th>FY09</th>
<th>FY10</th>
<th>FY11</th>
<th>FY12</th>
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R&D
($ in Billions)

24X Growth

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177X Growth in Operating Profit from 2009 → 2021
Moore’s Law Has Ended!

Physical Scaling Has Flattened

- Moore’s Law
- Logic Density
- Memory Density

Power Density Continues to Increase

Source: Broadcom data and estimates
Need New Approaches to Chip Development

- **General Purpose Compute**
- **Discrete Building Block Components**
- **Software Offload**
- **Analog Integration**
- **Domain Specific Silicon Accelerators**
- **Custom Silicon SoCs**

Are We on a New Growth Trajectory?
Frank Ostojic – SVP & GM, ASIC Products
Vijay Janapaty – VP & GM, Physical Layer Products
Foundation for Successful Silicon Innovation

Broadcom IP Portfolio + Leading Process Technology Platform
Custom ASICs Heritage, 3 Decades of Custom ASICs Experience

**Broadcom ASIC Products Division**

- The combination of 3 large ASIC groups: **Avago + LSI + Agere**
- Has been developing Custom Silicon for over **30 years** across **10+ technology generations** (0.35um to 3nm)
Custom ASIC Revenue by End Market

Routing / Switching
($ in Millions)

Compute Offload
($ in Millions)

20% CAGR
Custom ASIC Revenue by End Market

($ in Millions)

FY12 | FY13 | FY14 | FY15 | FY16 | FY17 | FY18 | FY19 | FY20 | FY21
--- | --- | --- | --- | --- | --- | --- | --- | --- | ---
$0 | $0 | $0 | $0 | $0 | $0 | $1,000 | $1,500 | $2,000 | $2,500

20% CAGR

- Compute Offload
- Routing/Switching
Broadest Silicon Capabilities

Architecture & Design
- System Knowhow
- Power Efficiency
- Design for Cost
- MCM/2.5D/3D Packaging
- Fast Ramp (NPI)
- Low DPPM Quality

Processing
- ARM CPUs
- DSP Cores
- Offload Engines
- Packet Processing
- Switching Cores
- Security Cores

Memory and Protocol
- Multiport SRAMs
- HBM I/F Cores
- DDR I/F Cores
- PCIe/CXL Cores
- SAS/SATA Cores
- Ethernet Cores

Signal Processing
- Analog VGA
- High Res ADC/DACs
- High-Rate ADC/DAC
- Modulation
- Filtering
- Error Correction

Connectivity
- PCIe SerDes
- SAS/SATA/FC SerDes
- Ethernet SerDes
- VSR SerDes
- MCM Chiplet
- High B/W Chiplet
Leading Edge Silicon Platform Cadence

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120 silicon tape outs per year (across all nodes, product lines)

Broadcom’s R&D Platform Scale Drives Innovation
Scale of the Broadcom ASIC Machine

- **Investment scale** enables the development of a new Technology **Platform** ~ every 2 years – in alignment with Foundry
- **R&D scale**, combined with **efficient design methodology**, enables the development of ~60 ASICs at a given time

- *Lead ASIC Tape-out*
- *Lead ASIC Production Release*

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<th>Year</th>
<th>16nm (90+ ASICs)</th>
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Proven Methodology for Very Complex SoCs

A Predictable ASIC Machine

- Designs in future generations will **double** current complexity
- Packaging and thermal technology leadership → **integration in complex SoCs**

Design Parameters
- Die sizes of 600 to 800 mm²
- 60B – 110B+ transistors in core die
- 96 GB – 128 GB of HBM capacity
- ~30 Tb – 50 Tb of network bandwidth
- Multiple die integrated in 2.5D packaging technology
Packaging Technology Leadership

Increasing SoC design content and size, coupled with a slowing of silicon area scaling, has led to a renaissance in packaging technology.

Evolution of 2D Packages

- **Small 40 mm x 40 mm Monolithic Package**
- **Large 60 mm x 60 mm Monolithic Package**
- **Super Large 80 mm x 80 mm Multi-die Package**

Evolution of 2.5D, 3D Packages

- **Si Interposer up to 1600 mm², Package Size 80 mm x 80 mm**
- **Si Interposer up to 3200 mm², Package Size 100 mm x 100 mm**
- **Si Interposer up to 3200 mm², Stacked Die, Package Size 100 mm x 100 mm**
Hyperscale Accelerator Examples

- General Purpose Compute
  - CPUs/GPUs
- Software Offload
- Domain Specific Silicon Accelerators
- Custom Silicon

New Growth Market for Custom Silicon
AI Custom Silicon

1. Matrix multiply/accumulate (5nm/3nm Libs/memories)
2. Network connectivity (800 Gbps/1600 Gbps links)
3. Die-to-die interconnect (10+ Tbit/s)
4. High bandwidth memory (HBM2e/3)
5. Advanced packaging (2.5D CoWoS)
6. First to market, fast NPI
Domain Specific Architectures Outperform GPUs/CPUs

Google TPU4: Speedup over NVIDIA A100

- BERT: 10%
- ResNet: 74%
- DLRM: 55%
- SSD: 41%

Source: cloud.google.com

Broadcom AI ASICs in Production

- 2018: 3
- 2020: 5
- 2022: 9

Source: Broadcom internal data

Higher Performance and 20%+ Lower Area and Power
Datacenter Accelerators

Benefits: Virtualization, Video, Protocol, Security Offloads and DC Orchestration

1. Virtualization, security, protocol offload (5nm/3nm)
2. Video codecs offload (5nm/3nm)
3. High bandwidth memory (HBM2e or DDR5)
4. CPU subsystem (ARM)
5. Network connectivity (800G links)

Hardware Accelerators Replace Software/CPU
Horizontal Integration

Discrete Building Block Components

Discrete Analog ICs from Non-CMOS or Older Generation CMOS

Analog Integration

Custom Silicon SoCs

Integrated Analog in Leading Process Technology Node

Integration Drives Content Growth
5G Radio: Bandwidth Increase, Power & Cost Reduction

• Integrated DFE and AFE
• Direct RF, DSP centric AFE
• 5G-advanced support
• BW > 800 MHz, dual-band TRXs
• 25%+ FE power reduction
• Antenna weight reduction
• Radio SKU reduction

5G Operator CapEx and OpEx Reduction

DFE = Digital Front End
AFE = Analog Front End
BW = Bandwidth
TRX = Transceiver
5G Massive MIMO Radio Silicon

1. Power efficiency (5nm/3nm libraries/memory)
2. Data converter chip-let (5nm direct RF, 5G-Adv, 800 MHz+)
3. Die-to-die interconnect (high bandwidth, low power chip-lets)
4. Protocol and control plane (Integrated ARM & DSP subsystems)
5. Baseband connectivity (CPRI, eCPRI interfaces)

First to Market: Direct RF Data Converters in 5nm

Custom 5G Radio SoC Opportunity = $1.2B SAM in CY24*

* Based on Dell'Oro January 2022 and Broadcom estimates
Data Center Interconnect: Integrated PAM-4 DSP

PAM-4 DSP Opportunity = $800M SAM in CY24*

Integration Centric

Discrete DSP, TIA, and Driver
Higher Power Dissipation

Integrated DSP Solution
400G DR4 Module < 7W
800G DR8 Module < 14W

Integration Drives 25% Power Reduction

* Based on LightCounting September 2021 and Broadcom estimates
Transport and Routing Network (Coherent DSP)

Discrete DSP and ADC/DAC Silicon
Limited Form Factors, Higher Power

Coherent DSP Opportunity = $400M SAM in CY24*

* Based on Broadcom estimates
Key Takeaways

Hyperscale accelerators offload software complexity to custom ASICs

Integration of discrete analog ICs drives custom silicon content growth

Broadcom is the #1 custom ASIC provider in infrastructure

Broadcom has a rich heritage of successful execution

– Breadth of IP cores + leading edge silicon platform + proven design methodology